PRACTICAL DESIGN OF C-BAND, MIC, PIN PHASE SHIFTERS

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Abstract

Characteristics of branch-line-hybrid coupled phase shift circuits were clarified using S-parameters, and 4-bit circuit simulation taking transmission-line losses into consideration was performed for the circuit optimization. Then the results were applied to C-band, MIC phase shifters. The simulation program was also utilized to estimate the effects of circuit parameter variations.

Introduction

In the previous design of MIC diode phase shifters, circuit optimization has not been discussed so much in terms of the insertion loss, phase shift error, input match and bandwidth.

This paper clarifies characteristics of the branch-line-hybrid coupled 180°-bit, and describes the circuit simulation taking microstrip transmission-line losses into account to realize the minimum insertion loss. Then the results are applied to C-band 4-bit MIC phase shifters for MLS of which schematic diagram is shown in Fig.1. Actual problems in circuit fabrication are also investigated using the simulation program.

Characteristics of branch-line-hybrid coupled bit

S-parameters offer the exact representation of a branch-line-hybrid coupled phase shift circuit shown in Fig.2. Port-2 and port-3 are loaded with reflecting terminations including pin diodes, of which reflection coefficients relative to the characteristic impedance of the coupler are Γ_1 and Γ_2 respectively. Defining port-1 as input and port-4 as output terminals, S-parameters of the branch-line-hybrid coupled phase shift circuit are expressed in matrix form,

$$S = S_A + S_B\Gamma(1 - S_A\Gamma)^{-1} S_B \qquad (1)$$

where submatrices of the S-parameters of the coupler[1] S_A, S_B and the reflection coefficient are defined as,

$$S_A = \begin{bmatrix} S_{11} & S_{41} \\ S_{41} & S_{11} \end{bmatrix} \qquad (2)$$

$$S_B = \begin{bmatrix} S_{21} & S_{31} \\ S_{31} & S_{21} \end{bmatrix} \qquad (3)$$

$$\Gamma = \begin{bmatrix} \Gamma_1 & 0 \\ 0 & \Gamma_2 \end{bmatrix} \qquad (4)$$

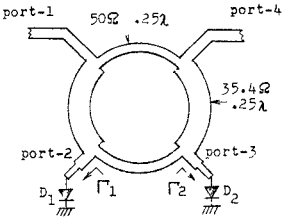


Fig.2 180° branch-line hybrid coupled phase shift circuit

At the center frequency of the coupler, where infinitely large isolation can be obtained between port-1 and port-4 ($S_{11}=S_{41}=0$), amplitude of the input reflection coefficient, r, and the transmission coefficient from port-1 to port-4, T, are reduced to,

$$r = |\Gamma_0| \cdot |S_{21}^2 + S_{31}^2| \qquad (5)$$

$$T = 2\Gamma_0 \cdot S_{21}S_{31} \qquad (6)$$

provided perfectly ballanced reactances ($\Gamma_1=\Gamma_2=\Gamma_0$) are connected. Then no reflection occurs at input and output, and change in phase of Γ_0, caused by switching the diodes, just coincides with the phase shift of the circuits. In this ideal case, optimization of the phase-matching network for a hybrid coupler phase shifter can be found in the literature[2].

Further investigation of Equation (1) instead of Equations (5) and (6) is required, when some extent of bandwidth is considered, as S_{11} and S_{41} are no longer zero. It reveals that $\angle\Gamma_0$ corresponding to two states of the diodes has important effects on the circuit performance.

In 180° phase shifter, switching the normalized loaded reactances from +j1 to -j1, for example, gives the least phase shift error, $\Delta\Psi$, but brings about rather abrupt increase in input mismatch. Switching them from j0 to j∞, on the other hand, produces just the opposite situation.

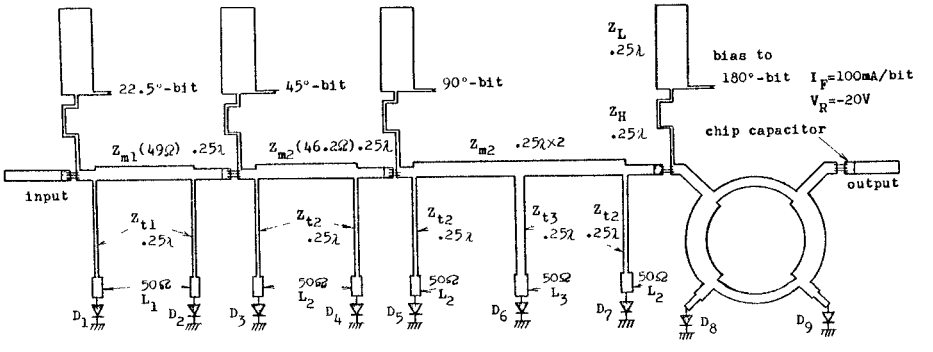


Fig.1 Schimatic diagram of a MIC 4-bit phase shifter circuit

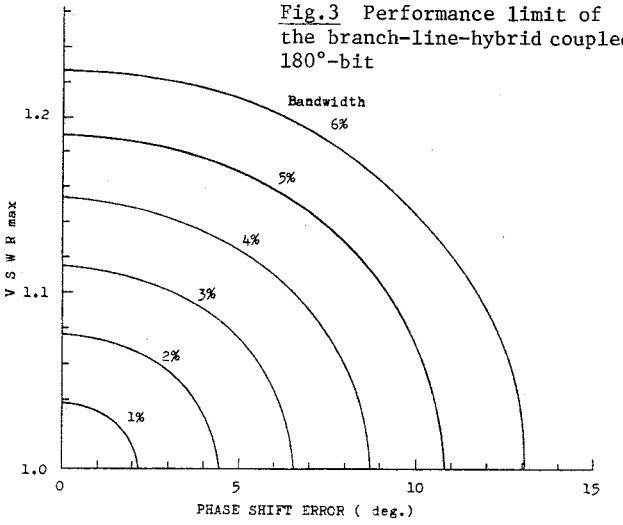


Fig.3 Performance limit of the branch-line-hybrid coupled 180°-bit

Correlation between input mismatch, $\Delta\Psi$ and bandwidth, B, is governed by $\angle\Gamma_0$ and expressed as,

$$(VSWR_{max}-1)^2 + (\Delta\Psi_{max})^2 = \frac{(1+\sqrt{2})^2\pi^2}{4} B^2 \qquad (7)$$

under some reasonable approximations. Equation (7) limits the performance of the branch-line-hybrid coupled 180°-bit, and requires a compromize between $VSWR_{max}$, $\Delta\Psi_{max}$ and B as shown in Fig.3.

In our phase shifter, circuit parameters are chosen so as to make $\Delta\Psi$ minimum. Diode junction capacitance, C_j, of 0.2 pF (R_s=0.6 ohm at 5 GHz, I_F= 50 mA) is the choice to realize the minimum insertion loss.

Optimum junction capacitance in loaded-line bit

Characteristic impedance of a $\lambda/4$ transmission-line, Z_m, and loading susceptance, B_0, in loadedline phase shift circuits are determined depending upon the phase shift, Ψ[3]. Parallal stubs composed of a $\lambda/4$ impedance transformer, a short 50 ohm transmission-line and a pin diode, connected in tandem, are conviniently used to transform the diode susceptance in both on- and off-state to $+B_0$ and $-B_0$.

Increasing C_j decreases both diode series, resistance, R_s, and characteristic impedance of the transformer, Z_t, then reduces loss due to transmission-line. As the rf power dissipation in the diode depends upon R_s relative to Z_t, calculation taking transmission-line losses into account gives optimum C_j. Propagation constant in microstrip transmission-lines given by Pucel et al. [4] was used for the calculation. Specific resistivity of our Cr-Au thin film system was assumed to be 3.2×10^{-6} ohm-cm[5].

In our design, where circuits are fabricated on a 0.635 mm thick alumina substrate, 0.3 pF (R_s=0.6 ohm at 5 GHz, I_F=50 mA) realizes the lowest loss in 22.5°- and 45°-bit. In three stub 90°-bit, changing C_j in the center stub to 0.2 pF increases bandwidth slightly although loss reduction is not expected.

Practical construction of the circuits and performance simulation

4-bit circuits shown in Fig.1 are fabricated on a 50.8x25.4 mm alumina substrate using Cr-Au microstrip transmission-lines, and packaged in a 63.2x40x 16 mm case with a conductive rubber gasket under the lid as shown in Fig.4.

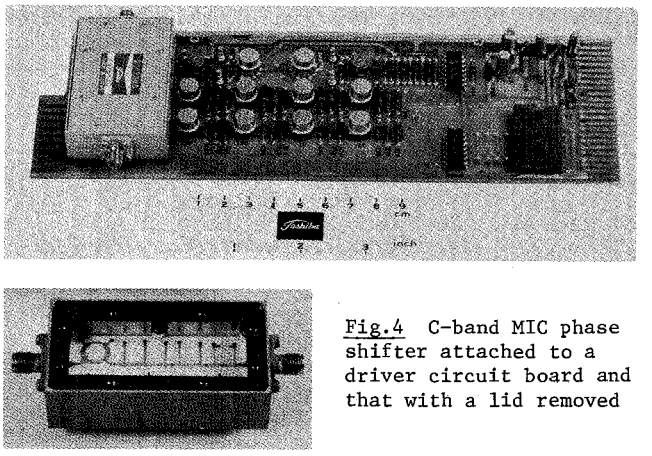


Fig.4 C-band MIC phase shifter attached to a driver circuit board and that with a lid removed

Diode chips mounted on gold-plated pedestals are installed in holes in the substrate and soldered to its ground metal as shown in Fig.5, where equivalent circuit of a mounted diode is shown as well. Chip capacitors used for dc and rf isolation are quivalent to a series circuit of a inductance (0.15 nH) and a resistance (0.9 ohm) at 5 GHz.

Performance of the 4-bit circuits can be readily expected by multiplying ABCD-parameters of simple unit circuits in order, whereby S-parameters of the branch-line coupled bit given by Equation (1) are transformed to ABCD-parameters. Fundamental building blocks for the 4-bit circuit calculation are listed in Fig.6.

In Fig.7 actual performance of the phase shifter is compared with the computer simulation over the frequencies of 5,000 to 5,120 MHz for 16phase states. Though VSWR and insertion loss, L_i, have similar characteristics in both cases, there is considerable difference in $\Delta\Psi$ as discussed in the next section. Losses due to transmission-lines (1.1 dB), diodes (0.4 dB), capacitors (0.4 dB) and mismatch (0.1 dB) result in maximum L_i of 2 dB.

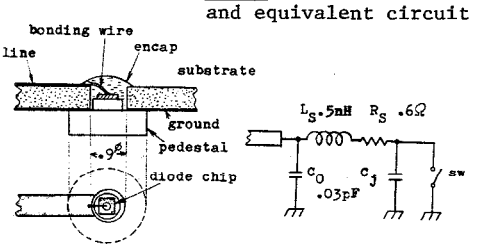


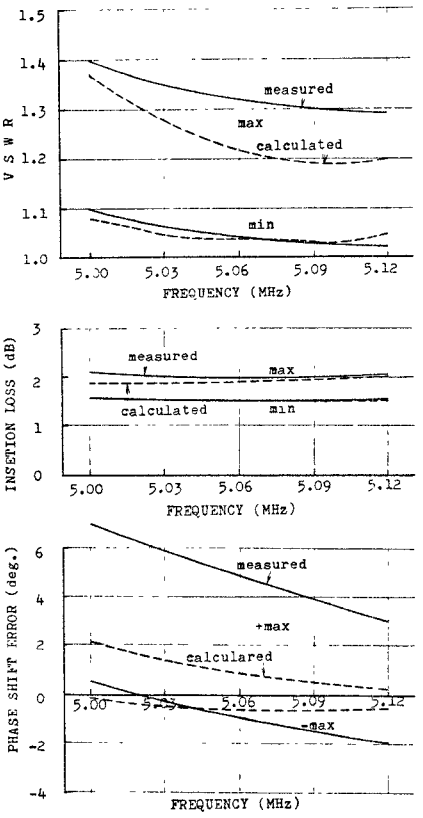
Fig.5 Diode mount structure and equivalent circuit

Origins increasing $\Delta\Psi$

There are three origins that increases $\Delta\Psi$, variations of C_j, variations of substrate thickness and dielectric constant, and lack of reproduceability to fix positions of diodes. How important effects do these exert on $\Delta\Psi$ can also be estimated by the simulation.

In planar-type pin diodes from the same wafer

Fig.7 (right) Measured and calculated performance of 4-bit phase shifters



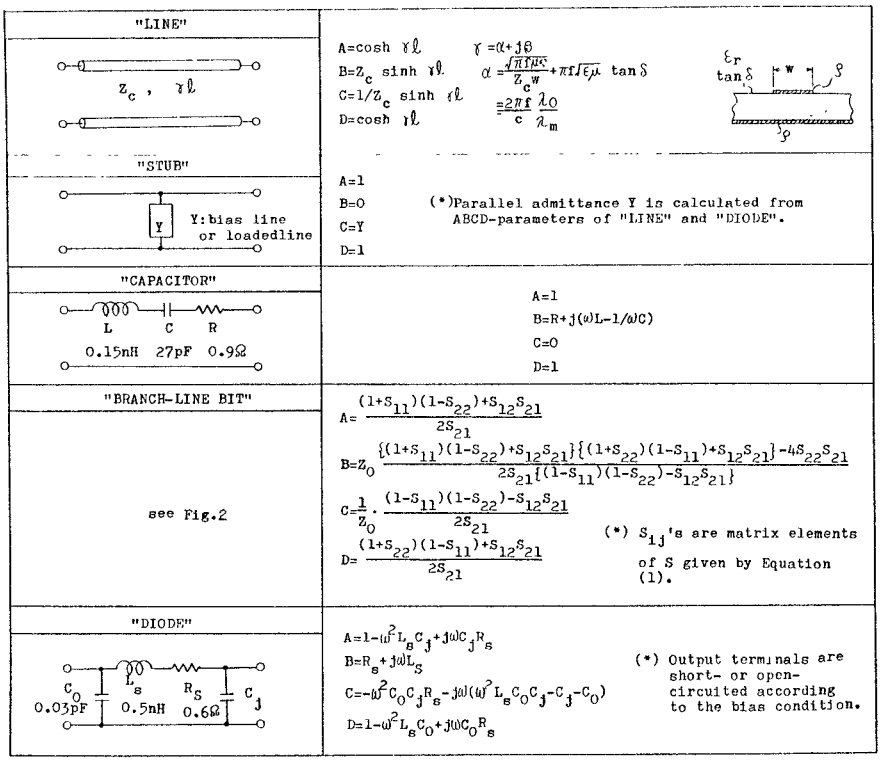


Fig.6 Fundamental building blocks of the 4-bit circuit and their ABCD-parameters

variations of C_j follow the normal distribution with standard deviation, σ, of 3.5 % in 0.2 pF diodes and 2.3 % in 0.3 pF diodes. If the circuits are well designed and adjusted to the average value of the distribution, there is no need to take the individual C_j into consideration. When chips from a different wafer are used, however, average C_j for the wafer must be kept within $\pm$3.5 % around the designed C_j to maintain $\Delta\Psi$ less than 6°. This is a rather strict requirement and may demand a little modification of the circuit parameters.

Almost similar discussion to C_j is made about the substrates. Variations of substrate thickness and dielectric constant should be kept within,

$$|\Delta h/h_0 - 0.989\Delta\varepsilon_r/\varepsilon_{r0}| \leq 0.079 \qquad (8)$$

where subscript 0 implies the value used in the design.

The last of three is troublesome and uncontrollable problem, depending upon the operator's carefulness and skillfulness. It is said from the simulation that, although shifting diode mount holes to shorten the stub has negligible effects on $\Delta\Psi$, shifting them to leave the edge of the stub increases inductance of the bonding wire, L_s, which in turn gives rise fairly large $\Delta\Psi$. Reproduceability of position of a diode chip on a pedestal, and that of a pedestal on the substrate, and the slack of the bonding wire also change L_s. Variations of L_s should be kept within $\pm$10 %.

Input match is not influenced so much by these variations.

Conclusions

Branch-line-hybrid coupled 180°-bit gives the least phase shift error when $\angle\Gamma_0$ is switched from +90° to -90°, although rather abrupt increase in input mismatch occurs. As transmission-line losses occupy more than half the insertion loss in MIC phase shifters, circuit simulation taking them into account is a necessary means to determine proper circuit parameters.

Circuit simulation shows, in addition, that great care should be taken of the structural identity around a diode mount not to increase $\Delta\Psi$. Except for this problem, actual characteristics of the C-band phase shifter agree well with the simulation.

Acknowledgment

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References

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